

1 **WHAT IS CLAIMED IS:**

2 1. An uninterruptible power supply comprising:
3 a controlled rectifier having an input coupled to receive AC power and an output
4 coupled to a DC bus;
5 a battery coupled to the DC bus;
6 an inverter having an input coupled to the DC bus and an output coupled to a
7 load; and
8 a control system coupled to the controlled rectifier and the inverter, the control
9 system comprising three microprocessors, wherein a first microprocessor
10 functions as an overall controller, a second microprocessor controls the
11 rectifier, and a third microprocessor controls the inverter.

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13 2. The uninterruptible power supply of claim 1 wherein the three microprocessors
14 communicate via a common global memory.

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16 3. The uninterruptible power supply of claim 2 further comprising a memory
17 arbitration circuit including a complex programmable logic device programmed to allow
18 priority-driven, non-preemptive access by the microprocessors to the common global
19 memory.

20
21 4. The uninterruptible power supply of claim 1 comprising a plurality of components
22 interconnected by a peer-to-peer controller area network, wherein the network
23 accommodates fragmented messaging.
24

1 5. The uninterruptible power supply of claim 1 further comprising a battery current
2 monitoring circuit comprising:

3 a current sensor disposed to monitor the battery current;

4 a first amplifier circuit receiving an output from the current sensor corresponding
5 to discharging battery current, amplifying it by a first factor, and
6 outputting it to the control system;

7 a second amplifier circuit receiving an output from the current sensor
8 corresponding to a charging battery current, amplifying it by a second
9 factor greater than the first factor, and outputting it to the control system;

10 wherein the control system selects as its input the output of the first amplifier
11 when the battery is discharging and the output of the second amplifier
12 circuit when the battery is charging.
13

14 6. The UPS of claim 1 having a three-phase input and independent zero-crossing
15 detection circuits for each input phase, wherein the second microprocessor independently
16 determines a phase shift introduced by each zero cross detection circuit and adjusts the
17 firing signal timing for each rectifier phase to negate the phase shift.
18

19 7. The UPS of claim 6 wherein the second microprocessor is configured to change
20 the firing sequence of the rectifier to compensate for a phase rotation of the three-phase
21 input.
22

23 8. The UPS of claim 6 wherein the second microprocessor qualifies the input voltage
24 by measuring the voltage on a first phase of said three-phase input, the frequency on a
25 second phase of said three-phase input, and the phase sequence between either said first
26 phase or said second phase and a third phase of said three-phase input.
27

28 9. The UPS of claim 1 wherein the second microprocessor implements a phase lock
29 loop for synchronizing rectifier firing, wherein the phase lock loop includes a finite
30 impulse response filter on the input voltages, thereby removing low frequency harmonics
31 from the input signal.

1
2 10. The UPS of claim 1 wherein the third microprocessor implements a nested control
3 loop having an inner loop and outer loop, said inner loop regulating inverter current using
4 a discrete sliding mode controller, and said outer loop regulating the inverter voltage
5 using a harmonic servomechanism controller.
6

7 11. A method of controlling the output current of a controlled rectifier having its
8 output connected to a DC bus with a battery coupled thereto, the method comprising:

9 sensing the DC bus voltage;

10 comparing the sensed voltage to a voltage setpoint;

11 increasing or decreasing the rectifier firing angle to minimize a difference
12 between the sensed voltage and the voltage setpoint;

13 determining whether an input current of the rectifier or a charging current of the
14 battery is above a predetermined limit; and

15 switching control to a different control loop to maintain the input current or the
16 charging current within the predetermined limit.
17

18 12. The method of claim 11 wherein the step of switching to a different control loop
19 includes pre-loading the integrator of the different control loop to prevent a discontinuity
20 in an output of the different control loop.
21

22 13. The method of claim 11 wherein the different control loop includes a non-linear
23 element.
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25 14. The method of claim 11, wherein on starting the rectifier, the voltage setpoint is
26 gradually increased from an initial value to a final value.
27

28 15. The method of claim 11 wherein the voltage setpoint is selected to cause a
29 particular charging current to flow into said battery.
30

1 16. The method of claim 15 wherein the voltage setpoint is selected from one of a
2 higher value to accomplish faster charging or a lower value to accomplish slower
3 charging.

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5 17. The method of claim 15 wherein the voltage setpoint is selected to cause zero
6 charging current to flow into said battery.

7

8 18. The method of claim 15 wherein the voltage setpoint is selected as a function of
9 battery temperature.

10

11 19. A method of operating a plurality of uninterruptible power supplies in parallel
12 comprising:

13 adjusting a phase angle of a voltage generated by each uninterruptible power
14 supply to eliminate real power unbalances among the plurality of
15 uninterruptible power supplies;

16 adjusting a magnitude of a voltage generated by each uninterruptible power
17 supply to eliminate reactive power unbalances among the plurality of
18 uninterruptible power supplies; and

19 shifting a location of a harmonic servo compensator pole to reduce the bandwidth
20 of the controller for each harmonic.